Design of Class A/AB Amplifier

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ABSTRACT

This paper presents fully differential operational trans-conductance amplifier (OTA) for switched capacitor circuits with very low voltage and quick settling is presented using two stage class A/AB amplifier. Active current mirrors serve as the second stage of the proposed two-stage OTA, a hybrid class A/AB device that uses a folded cascade as the first stage. Two-stage, class A/AB operational amplifiers are used to achieve precise control of common-mode levels, good power supply noise rejection, and low power dissipation. Slew limitation only happens in the first stage as a result of the second stage operating in class AB, which reduces the power dissipation for switched-capacitor circuits. Additionally, the cascode compensation mechanism is used for quick settlement. The two-stage class A/AB amplifier is as a component of an audio sigma-delta modulator applications. This OTA fuses a straightforward differential pair as the initial stage, with current flow the second step being mirrors. The class AB operation in the second stage that causes the slew limiting only occur in the first stage. Thus, it lowers static power consumption. The power consumption of the class A/AB amplifier is 36uW from 1V supply voltage the GBW value of the class A/AB operational amplifier is 45MHz and the Gain is 56dB.

Keywords: Amplifier, DC gain, GBW, Class A/AB

1. INTRODUCTION

A analog circuit is challenging to design. The amplifier design required at the front of almost all analog front end. A class A/AB amplifier is design in Cadence for multi-bit delta-sigma modulator. The amplifier can achieve 56dB with GBW of 45 MHz and unit gain frequency of. The complete simulation shows that amplifier can get 36 µW at supply voltage of 1-V.The operational amplifier (Op-amp) is one of the essential building blocks in analog integrated circuits. It is widely used in sample and hold block, analog-to-digital (A/D) and digital-to-analog (D/A) converters, switched-capacitor filters, voltage references, etc. The proposed two-stage OTA is a hybrid class A/AB that combines a folded cascode as the first stage with active current mirrors as the second stage. The performance of an Op-amp is evaluated by some characteristics such as unity gain frequency , phase margin, open-loop gain, and input-referred noise . Power consumption is one of the most challenging issues in modern portable electronic equipment. Reduction of the power dissipation looks even more challenging in low-voltage analog integrated circuits, as there will be less room for the signal and to keep the same signal-to-noise ratio, the power is to be

increased. The power consumption is also increased when the operating speed is increased. Therefore, low-power design approaches for low-voltage fast-settling operational amplifiers in switched-capacitor applications can be very attractive.

2. OPERATIONAL AMPLIFIER

The operational amplifier using in third order delta-sigma modulator so the first integrator determines the overall noise and linearity of the modulator. The circuit schematic of the op-amp is shown in Fig(1). It is a two-stage design, with a class-AB second stage and a first stage that uses a pmos input pair with large channels to reduce input-referred noise. According to Fig. 1(a), the op-amp is Miller-compensated utilising Rz and Cc 150 fF is chosen as the value of Cc The in-band noise caused by op-amp nonlinearity can be reduced more effectively with a two-stage design than a single-stage op-amp, it can be demonstrated. The CMFB circuit that stabilizes the output level of the first stage is shown in Fig. 1(b). The quiescent output voltage at nodes o1p and o1m (which is also the gate–source voltage of M6–M61 and M8–M81) sets the quiescent currents in the second stage. To set the output quiescent currents accurately, the common-mode reference vref is derived from a diode-connected transistor biased with a fixed current. Since the signal swings at o1p and o1m are modest, the linearity of the common-mode detector is not critical. The 70 fF capacitors bypass the active common-mode detector for high frequencies and help stabilize the loop. The first stage uses a 2.8 uA tail current. Since the output swings of the op-amp are large, linear operation of the CMFB mechanism is ensured by using resistive averaging to detect the output common mode [Fig. 1(c)]. The 250 fF capacitors provide a fast high-frequency path, bypassing the resistive common-mode detector and the error amplifier. At high frequencies, where the compensation C capacitors can be considered as shorts, the common-mode output impedance of the op-amp in Fig. 1(a) consists of the parallel combination of the positive resistance of the diode-connected (through C_C) transistors M8 and M81 and the negative resistance formed by the loop M6-M4-M7 and M61-M41-M71. If equal quiescent currents are used in M8 and M7, this impedance is infinite. In the presence of mismatches, it is possible for the common-mode output impedance to have a negative real part and lead to instability. To prevent this, quiescent currents in the lower transistors M8 and M81, which contribute to the positive resistance, are made 1.5 times larger than quiescent currents in the upper transistors M7 and M71. The remainder of the quiescent current is provided by the CMFB circuitry. This technique ensures stability and reliable operation of the CMFB loop. Quiescent current through each output branch (M8 and M81) is 1.2 A. The two stage class A/AB amplifier used in different circuit due to best parameter values such as, Dc gain ,GBW ,phase margin . The two stage class A/AB amplifier used in third-order delta-sigma (ADC) achieve good performance such as SNR ,SNDR ,86 dB . The effective number of bit (ENOB) is 14 bit.

2. ARCHETECTURE

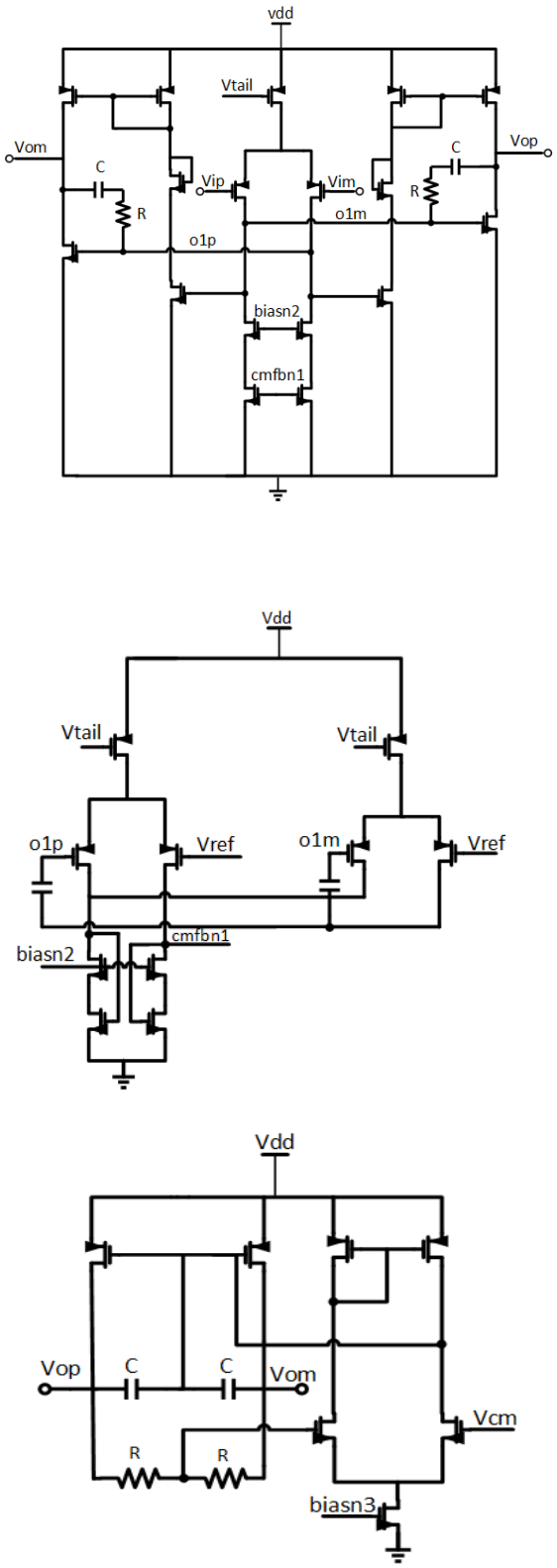

Figure 1: Class A/AB amplifier (a) Common feedback circuit (b) and (c).

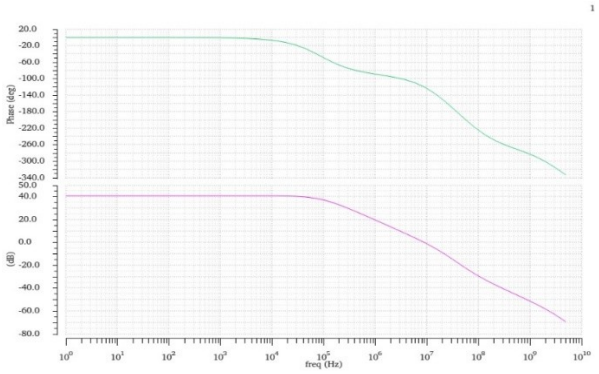

Figure 2: Open loop gain of op-amp

Table I : Results of class A/AB amplifier

Parameters	Values
Gain (dB)	56
GBW (MHz)	45
Power (uW)	36
Phase margin	73
Offset voltage (mV)	15
Dc gain(dB)	53

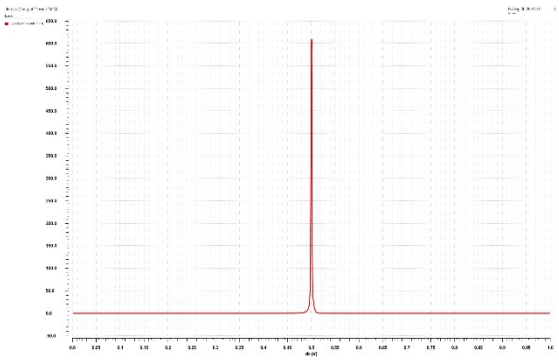

Figure 3: Dc Gain of Op-amp

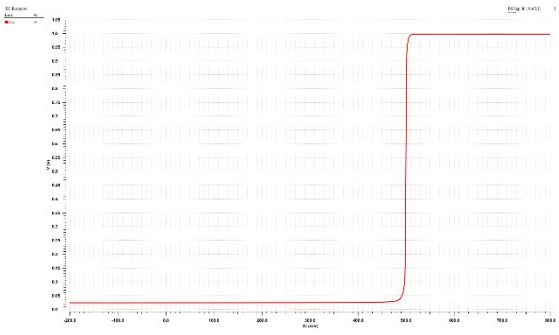

Figure 4: Offset voltage of Op-amp

4. CONCLUSION

A class A/AB amplifier is designed in Cadence to trade-off the performance and power consumption. The circuit simulation shows it can achieve higher DC gain of 56-dB. The amplifier GBW is quite higher and very useful for the many data conversion techniques

5. ACKNOWLEDGMENT

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6. REFERENCES

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